REMARKS

Claims 1-14 are currently pending.

Applicant appreciates the Patent Office's indication that claim 5 has allowable subject matter, but believes that all pending claims are allowable over the prior art of record.

The Patent Office asserted (page 5, lines 10-18, of the Final Office Action mailed February 28, 2006) "As per the first argument, Horng teaches that the chip identification number are generated in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device and [see column 4, lines 34-62.] Furthermore, the examiner would like to point out that determining address/ID based on the order of the bits in one or more data word is well known in the computer art, please see pages 622-624 of the "Logic and Computer Design Fundamentals" by M. Morris Mano and Charles R. Kime. Figure 14-3 shows that the order of bits in a word determines the address."

Applicant, as discussed here and below, asserts that Horng does not teach "an identity acquisition unit ... in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..." Where in Horng is there reference to the use of the order of receipt of bits of one or more data words? The claims recite that "in response to the order in which the bits of one or more data words of a predetermined form are received" the "identity acquisition unit" determines "an identity of the device." In Horng (column 4, lines 21-24) discloses that Lofstrom, U.S. Patent No. 6161213, incorporated by reference by Horng, discloses producing a chip ID by an ID generation circuit. In Lofstrom, the chip ID is determined through measurements, as shown in figure 8, in which the sources of paired FETs 62 are supplied from a positive power supply rail 106 in which switching of the FETs occurs through a common ROW select bit line 60 (column 7, lines 19-54, of Lofstrom). Lofstrom does not appear to disclose or fairly suggest teach "an identity acquisition unit ... in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..."

Applicant requests that the Patent Office point out with particularity where Horng discloses "an identity acquisition unit ... in response to the order in which the bits of one or more

data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..." and other claim limitations.

Applicant has reviewed pages 622-624 of "Logic and Computer and Design Fundamentals," by M. Morris Mano and Charles R. Kime. These pages appear to disclose virtual memory and mapping main memory to cache memory, but does not appear to disclose "an identity acquisition unit ... in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..." or other claim limitations.

Thus, applicant believes that all pending claims are allowable over the prior art of record.

Continuing with the Patent Office's Final Office Action, pages 2-4, mailed February 28, 2006, the Patent Office has rejected claims 1-14 under 35 U.S.C. 103(a) as being unpatentable over Horng, et al., U.S. Patent No. 6,738,788, and further in view of Dabral, et al., U.S. Patent No. 6,192,431.

Claim 1 recites "A data handling apparatus capable of operating in a system in which two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and each of the two or more devices having two or more data bus connectors, each for connection to a respective data line of the data bus; **an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device**; and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination."

Claim 9 recites "A data handling system comprising two or more data handling devices, each of the two or more data handling devices comprising a data bus; two or more data bus connectors, each for connection to a respective data line of the data bus; **an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the**

first mode of operation determine an identity for the device and store the identity in an identity store of the device; and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination."

Claim 13 recites "A method for assigning an identity to each of two or more devices of a data handling apparatus capable of operating in a system in which said two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and the device having two or more data bus connectors, each connected to a respective data line of the data bus, the method comprising in a first mode of operation of the device, receiving data transmitted over the data bus and **in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device**; and storing the identity in an identity store of the device."

The Patent Office asserted (page 2, lines 16-21, of the Office Action mailed February 28, 2006) "an identity acquisition unit [see column 4, lines 52-62 and figure 1, element 12] capable of functioning in a first mode of operation of the device to received data transmitted over the data bus and in response to the order in which the bits or one or more data words are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device [see column 4, lines 34-62]."

Horng recites (column 4, lines 16-62)

> The present invention relates to computer readable media storing software which, when read and executed by a conventional computer, **causes the computer to implement a database engine that keys data records to a binary number which may have randomly-positioned, non-deterministic bits. The chip ID produced by the ID generation circuit described in the aforementioned U.S. Pat. No. 6,161,213 (incorporated herein by reference) is an example of such a number.** Suitable computer-readable media for storing the software include, but are not limited to, compact disks, floppy disks, hard disks, and random access or read only memory. While the specification describes an exemplary embodiment and application of the invention considered by the applicants to be a best mode of practicing the invention, it is not intended that the invention be limited to the exemplary embodiment or to the application described below.
> FIG. 1 is a data flow diagram illustrating an exemplary data acquisition, storage and retrieval system 8 in accordance with the invention for storing and retrieving data relative

> to an IC chip (or die) 10 producing a unique ID. In the example of FIG. 1, each IC chip 10 suitably produces a 256-bit binary ID, comprising a 32-bit typeID and a 244-bit uniqueID as a key. However it should be understood that database systems in accordance with the invention may employ keys of other lengths and may be useful in contexts other than a chip identification system. The typeID field is identical for all ICs 10 of the same type, and all bits of the typeID field are deterministic, in that the ID generation circuit sets them to the same fixed values every time it generates the ID. The uniqueID field contains a number that is unique to each IC chip 10 even though a small percentage of its bits may be non-deterministic, in that the ID generation circuit may not always set them to the same value each time it generates a chip ID.
> System 8 includes a data acquisition system 12 such as, for example, an integrated circuit tester or any other device suitable for reading the chip ID generated by the ID generation circuit within IC chip 10. System 8 also includes a hierarchical database engine 14 in accordance with the invention for maintaining a separate "chip-type" database 16 for each possible value of the typeID field of the ID generated by IC chip 10. Database engine 14 is preferably implemented by a conventional computer programmed via software stored on computer-readable media that the conventional computer reads and executes.

Horng discloses (column 4, lines 21-24) U.S. Patent No. 6,163,213, as an example of determining a chip ID by randomly positioned, non-deterministic bits. The first paragraph in the summary of the invention of U.S. Patent No. 6,163,213, recites:

> **An integrated circuit identification (ICID) circuit** in accordance with one aspect of the invention produces a unique identification number or record (ID) for each chip in which it is included even though the ICID circuit is fabricated on all chips using identical masks. The ICID circuit includes a set of circuit cells and **produces its output ID based on measurements of outputs of those cells that are functions of random parametric variations that naturally occur when fabricating chips.** When the number of cells is large enough, each of millions of chips can be provided with a unique identifying ID without having to customize each chip.

Apparently, Horng generates a chip identification number or code from measurements of internal chip components and not "in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device." Dabral does not remedy this deficiency of Horng since Dabral teaches a pinout may be selected (Figure 1a) by biasing a configuration I/O port to either power or ground (column 4, lines 13-26). Thus, Horng and Dabral, alone or in combination, do not make obvious claims 1-14.

Claim 2 recites "wherein the identity acquisition unit is arranged to process each of the one or more data words of a predetermined form in accordance with a look-up table in order to

determine the identity for the device." As to claim 2, Horng (column 4, lines 34-62) does not appear to disclose or fairly suggest a lookup table. A hierarchical database engine is not a lookup table. Thus, claim 2 is allowable over the prior art of record for this additional reason.

The Patent Office asserted (last four lines of the Final Office Action mailed February 28, 2006) "As per the second argument, Horng teaches wherein the identity acquisition unit is arranged to process the or each data word of a predetermined form in accordance with a look-up table in order to determine the identity for the device [see Horng column 4, lines 34-62, 'database' and column 3, lines 42-49, 'database system'.]

Applicant submits that a database is not a lookup table nor is a database system a lookup table. From http://en.wikipedia.org/wiki/Associative_array, "An **associative array** (also known as a map, lookup table, or dictionary and in query-processing as an index or index file) is an abstract data type composed of a collection of keys and a collection of values, where each key is associated with one value. The operation of finding the value associated with a key is called a *lookup* or indexing, and this is the most important operation supported by an associative array. The relationship between a key and its value is sometimes called a mapping or binding. For example, if the value associated with the key "bob" is 7, we say that our array *maps* "bob" to 7. Associative arrays are very closely related to the mathematical concept of a function with a finite domain..."

According to Wikipedia's definition of a database, http://72.14.203.104/search?q=cache:LORcdd1Nj6cJ:en.wikipedia.org/wiki/Database+wikipedia+database&hl=en&gl=us&ct=clnk&cd=1 , "A database is an organized collection of data. The term originated within the computer industry, but its meaning has been broadened by popular use, to the extent that the European Database Directive (which creates intellectual property rights for databases) includes non-electronic databases within its definition. This article is confined to a more technical use of the term; though even amongst computing professionals, some attach a much wider meaning to the word than others."

Horng does not disclose or fairly suggest a lookup table. The term "key," as referred to by Horng (column 4, lines 34-62) is formed of a typeID and the generated unique ID.

Applicant thanks the Patent Office for the indication of allowable subject matter in claim 5.

The Patent Office is respectfully requested to reconsider and remove the rejections of the claims 1-4 and 6-14 under 35 U.S.C. 103(a) based on Horng and Dabral, and to allow all of the pending claims 1-14 as now presented for examination. An early notification of the allowability of claims 1-14 is earnestly solicited.

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Respectfully submitted:

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